

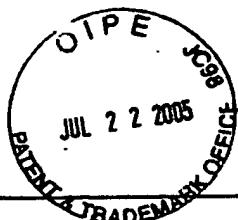


**\* EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 of 27

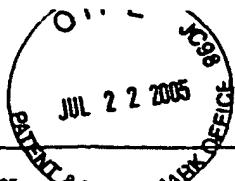
JUL 22 2005  
PATENT & TRADEMARK OFFICE  
FCB

FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE				ATTORNEY DOCKET NO.	APPLICATION NO.		
				MP0020	09/737,7433		
LIST OF REFERENCES CITED BY APPLICANT				APPLICANT			
				Sehat SUTARDJA			
DATE SUBMITTED TO USPTO: July 22, 2005				FILING DATE	GROUP		
				12/18/2000	2631		
U.S. PATENT DOCUMENTS							
*EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
P	2002/0136321	09/2002	CHAN				
	2003/0002570	01/2003	CHAN				
	2004/0005015	01/2004	CHAN				
	2004/0090981	05/2004	LIN, et al.				
	2004/0091071	05/2004	LIN, et al.				
	2004/0105504	06/2004	CHAN				
↓	2005/0025266	02/2005	CHAN				
	60/406,265	10/30/1998	CHAN				
W	4,131,767	12/1978	WEINSTEIN				
	5,323,157	06/1994	LEDZIUS, et al.				
	6,185,263	02/2001	CHAN				
	6,259,680	07/2001	BLACKWELL, et al.				
	6,259,745	07/2001	CHAN				
	6,373,908	04/2002	CHAN				
	6,389,077	05/2002	CHAN				
	6,4111,647	06/2002	CHAN				
	6,509,857	01/2003	NAKAO				
	6,594,304	07/2003	CHAN				
	6,690,742	02/2004	CHAN				
↓	6,744,831	06/2004	CHAN				
EXAMINER <i>phuong phu</i>				DATE CONSIDERED	9/13/05		
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							
2 of 27							



**\* EXAMINER:** Indicate reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

3 of 27



FORM PTO 1449 MODIFIED  
U.S. PATENT AND TRADEMARK OFFICE

### LIST OF REFERENCES CITED BY APPLICANT

DATE SUBMITTED TO USPTO: July 22, 2005

ATTORNEY DOCKET NO.	APPLICATION NO.
MP0020	09/737,743
APPLICANT	
Sehat SUTARDJA	
FILING DATE	
12/18/2000	2631

### U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
ff	3,543,009	11/1970	VOELCHER, JR.			
	4,112,253	09/1978	WILHELM			
	4,152,541	05/1979	YUEN			
	RE30,111	10/1979	BLOOD, JR.			
	4,362,909	12/1982	SNIJDERS, et al.			
	4,393,494	07/1983	BELFORTE, et al.			
	4,727,566	02/1988	DAHLQVIST			
	4,888,762	12/1989	ARAI			
	4,935,919	06/1990	HIRAGUCHI			
	4,947,171	08/1990	PFIEFER, et al.			
	4,999,830	03/1991	AGAZZI			
	5,222,084	06/1993	TAKAHASHI			
	5,305,379	04/1994	TAKEUCHI			
	5,307,405	04/1994	SIH			
	5,357,145	10/1994	SEGARAM			
	5,388,092	02/1995	KOYAMA, et al.			
	5,418,478	05/1995	VAN BRUNT, et al.			
	5,517,435	05/1996	SUGIYAMA			
	5,539,773	07/1996	KNEE, et al.			
	5,596,439	01/1997	DANKBERG, et al.			
	5,625,357	04/1997	CABLER			
	5,651,029	07/1997	YANG			
	5,659,609	08/1997	KOIZUMI, et al.			
	5,663,728	09/1997	ESSENWANGER			
	5,666,354	09/1997	CECCHI, et al.			
	5,796,725	08/1998	MURAOKA			
	5,822,426	10/1998	RASMUS, et al.			
	5,825,819	10/1998	COGBURN			

EXAMINER

phung phu

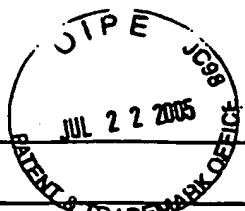
DATE CONSIDERED

9/13/05

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

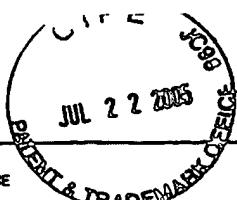


**\*EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



**EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

6 of 27



FORM PTO 1449 MODIFIED  
U.S. PATENT AND TRADEMARK OFFICE

LIST OF REFERENCES CITED BY APPLICANT

DATE SUBMITTED TO USPTO: July 22, 2005

ATTORNEY DOCKET NO.	APPLICATION NO.
MP0020	09/737,743
APPLICANT	
Sehat SUTARDJA	
FILING DATE	GROUP
12/18/2000	2631

U.S. PATENT DOCUMENTS

*EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
✓	4,746,903	05/1988	CZARNIAK, et al.			
	5,043,730	08/1991	OBINNATA			
	5,465,272	11/95	SMITH			
	5,471,665	11/95	PACE, et al.			
	5,489,873	02/96	KAMATA, et al.			
	5,508,656	04/96	JAFFARD, et al.			
	5,517,141	05/96	ABDI, et al.			
	5,539,405	07/1996	NORSWORTHY			
	5,572,158	11/96	LEE, et al.			
	5,585,795	12/1996	YUASA, et al.			
	5,587,681	12/96	FOBBESTER			
	5,648,738	07/97	WELLAND, et al.			
	5,663,728	09/1997	ESSENWANGER			
	5,757,219	05/98	WEEDON, et al.			
	5,760,726	06/1998	KOIFMAN, et al.			
	5,798,664	08/98	NAGAHORI, et al.			
	5,844,439	12/98	ZORTEA			
	5,880,615	03/99	BAZES			
	5,940,442	08/99	WONG, et al.			
	6,043,766	03/00	HEE, et al.			
	6,044,489	03/00	HEE, et al.			
	6,121,831	09/00	MACK			
	6,140,857	10/00	BAZES			
	6,148,025	11/00	SHIRANI, et al.			
	6,163,283	12/2000	SCHOFIELD			
	6,188,282	02/01	MONTALVO			
	6,204,788	03/2001	TANI			
✓	6,236,346	05/2001	SCHOFIELD			

EXAMINER

Phuong phu

DATE CONSIDERED

9/13/05

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

70827



FORM PTO 1449 MODIFIED  
U.S. PATENT AND TRADEMARK OFFICE

ATTORNEY DOCKET NO.	APPLICATION NO.
MP0020	09/737,743

### LIST OF REFERENCES CITED BY APPLICANT

DATE SUBMITTED TO USPTO: July 22, 2005

APPLICANT	GROUP
Sehat SUTARDJA	2631

### U.S. PATENT DOCUMENTS

*EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
W	6,275,098	08/01	UEHARA, et al.			
	6,288,604	11/01	SHIH, et al.			
	6,433,608	08/02	HUANG			
	6,509,857	01/2003	NAKAO			
	6,882,216	04/05	KANG			
✓	2002/0181601	12/02	HUANG, et al.			

### FOREIGN PATENT DOCUMENTS

*EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION OR ABSTRACT
W	EP 0 800 278	08/1997	EUROPE			
	JP 57-48827	3/1982	JAPAN			
	JP 204527	8/1989	JAPAN			
✓						

### OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)

W	Bertolaccini, Mario, et al., "A Precision Baseline Offset and Drift Corrector for Low-Frequency Applications," IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT, Vol. IM-34, No. 3, September, 1985, pp. 405-412.
W	Everitt, James, et al., "A CMOS Transceiver for 10-Mb/s and 100-Mb/s Ethernet," IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. 33, No. 12, December 1998, pp. 2169-2177.
	Kelly, N. Patrick, et al., "WA 18.5 - A Mixed-Signal DFE/FFE Receiver for 100Base-TX Applications," ISSCC 2000/SESSION 18/WIRELINE COMMUNICATIONS/PAPER WA 18.5, 2000 IEEE International Solid-State Circuits Conference, pp. 310-311.
	Song, Bang-Sup, et al., "FP 12.1: NRZ Timing Recovery Technique for Band-Limited Channels," ISSCC 96/SESSION 12/SERIAL DATA COMMUNICATIONS/PAPER FP 12.1, 1996 IEEE International Solid State Circuits Conference pp. 194-196.
	LINEAR TECHNOLOGY, High Speed Modem Solutions, InfoCard 20, Linear Technology Corporation.
	LINEAR TECHNOLOGY, LT1355/LT1356, Dual and Quad 12MHz, 400V/us Op Amps, Linear Technology Corporation, pp. 1-16.
	LINEAR TECHNOLOGY, LT1358/LT1359, Dual and Quad 25MHz, 600V/us Op Amps, Linear Technology Corporation, pp. 1-12.
	LINEAR TECHNOLOGY, LT1361/LT1362, Dual and Quad 50MHz, 800V/us Op Amps, Linear Technology Corporation, pp. 1-12.
	LINEAR TECHNOLOGY, LT1364/LT1365, Dual and Quad 70MHz, 1000V/us Op Amps, Linear Technology Corporation, pp. 1-12.
✓	LINEAR TECHNOLOGY, LT1813/LT1814, Dual/Quad 3mA, 100MHz, 750V/us Operational Amplifiers, Linear Technology Corporation, pp. 1-16.

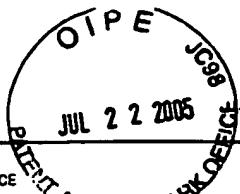
EXAMINER

DATE CONSIDERED

9/13/05

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

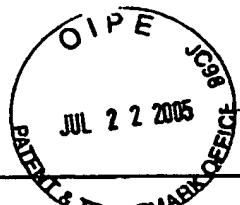
80527



**EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

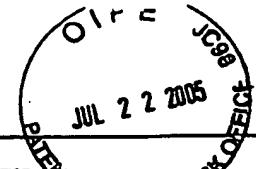
9 of 27





**EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

11 of 27



FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE		ATTORNEY DOCKET NO.	APPLICATION NO.
		MP0020	09/737,743
LIST OF REFERENCES CITED BY APPLICANT		APPLICANT	
		Sehat SUTARDJA	
DATE SUBMITTED TO USPTO: July 22, 2005		FILING DATE	GROUP
		12/18/2000	2631

#### FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION OR ABSTRACT
MP	63-300700	12/07/1988	Japan			
	06-97831	04/08/1994	Japan			
	06-97831	04/20/2005	Japan			Yes
	05-064231 A	03/12/1993	Japan			
	06-029853	02/04/1994	Japan			
	09-55770	08/17/1995	Japan			
	09-55770	08/17/1995	Japan			Yes
	09-270707	03/03/1996	Japan			
	09-270707	04/19/2005	Japan			Yes
	2001-177409	12/16/1999	Japan			
✓	2001-177409	04/20/2005	Japan			Yes

#### OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)

MP	Johns, et al., "Integrated Circuits for Data Transmission Over Twisted Pair Channels", March, 1997, pgs. 398-406.
	"IEEE Standard 802.3: Part 3 Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Detection", March 8, 2002, pgs. 1-378.
	Young, et al., "A Low-Noise RF Voltage-Controlled Oscillator Using On-Chip High-Q Three-Dimensional Coil Inductor and Micromachined Variable Capacitor", June 8-11, 1998, pgs. 128-131.
	Young, et al., "A Micromachined Variable Capacitor for Monolithic Low-Noise VCOS", 1996, pgs. 86-89.
	Abidi, et al., "FA 7.2: The Future of CMOS Wireless Transceivers", February 7, 1997, pgs. 118-119, 440.
	Eto, et al., "A 333 MHz, 20mW, 18ps Resolution Digital DLL using Current-controlled Delay with Parallel Variables Resistor DAC (PVR-DAC)", August 28-30, 2000, pgs. 349-350.
	Harald, et al., "Design of a 10-bit 100 MSamples/s BiCMOS D/A Converter", 1996, pgs. 730-733.
	Lee, et al., "A 3V 10b 100MS/s DIGITAL-TO-ANALOG CONVERTER FOR CABLE MODEM APPLICATIONS", August 28-30, 2000, pgs. 203-205.
	Henriques, et al., "A CMOS Steering-Current Multiplying Digital-to-Analog Converter", 1995, pgs. 145-155.
	Wikner, et al., "Modeling of CMOS Digital-to-Analog Converters for Telecommunication", May, 1999, pgs. 489-499.
	Van der Plas, et al., "A 14-Bit Intrinsic Accuracy $Q^2$ Random Walk CMOS DAC", December, 1999, pgs. 1708-1718.
	Radke, et al., "A 14-Bit Current-Mode $\Sigma\Delta$ DAC Based Upon Rotated Data Weighted Averaging", August, 2000, pgs. 1074-1084.
✓	Shui, et al., "Mismatch Shaping for a Current-Mode Multibit Delta-Sigma DAC", March, 1999, pgs. 331-338.

EXAMINER	MPJLW	DATE CONSIDERED	9/13/05
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			



FORM PTO 1449 MODIFIED  
U.S. PATENT AND TRADEMARK OFFICE

### LIST OF REFERENCES CITED BY APPLICANT

DATE SUBMITTED TO USPTO: July 22, 2005

ATTORNEY DOCKET NO.	APPLICATION NO.
MP0020	09/737,743
APPLICANT	
Sehat SUTARDJA	
FILING DATE	GROUP
12/18/2000	2631

### U.S. PATENT DOCUMENTS

*EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
W	6,259,957 B1	07/10/2001	Alexander, et al.			
	6,452,428 B1	09/17/2002	Mooney, et al.			
	5,745,564	04/28/1998	Meek			
	5,399,996	03/21/1995	Yates, et al.			
	5,887,059	03/23/1999	Xie, et al.			
	5,185,538	02/09/1993	Kondoh, et al.			
	5,204,880 (A)	04/20/1993	Wurster, et al.			
	5,272,453	12/21/1993	Traynor, et al.			
	5,325,400	06/28/1994	Co, et al.			
	5,440,514	08/08/1995	Flannagan, et al.			
	5,440,515	08/08/1995	Chang, et al.			
	5,479,124	12/26/1995	Pun, et al.			
	5,559,476	09/24/1996	Zhang, et al.			
	5,568,064	10/22/1996	Beers, et al.			
	5,600,321	02/04/1997	Winen			
	5,687,330	11/11/1997	Gist, et al.			
	5,757,298 (A)	05/26/1998	Manley, et al.			
	5,798,661	08/25/1998	Runaldue, et al.			
	5,838,177 (A)	11/17/1998	Keeth			
	5,999,044	12/07/1999	Wohlfarth, et al.			
	6,052,076	04/18/2000	Patton, III, et al.			
	6,057,716	05/02/2000	Dinteman, et al.			
	6,166,572	12/26/2000	Yamoaka			
	6,721,379 B1	04/13/2004	Cranford, Jr., et al.			
	5,859,552	01/12/1999	Do, et al.			

EXAMINER

Plumyplu

DATE CONSIDERED

9/13/05

\* EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

13 of 27



FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE		ATTORNEY DOCKET NO.	APPLICATION NO.
		MP0020	09/737,743
LIST OF REFERENCES CITED BY APPLICANT		APPLICANT	
		Sehat SUTARDJA	
DATE SUBMITTED TO USPTO: July 22, 2005		FILING DATE	GROUP
		12/18/2000	2631

#### FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION OR ABSTRACT

#### OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)

✓	Weaver, Jr., "A Third Method of Generation and Detection of Single-Sideband Signals," December 1956, pp. 1703-1705.
	Niknejad et al., "Analysis and Optimization of Monolithic Inductors and Transformers for RF ICs," 1997, pp. 375-378.
	Weigandt et al., "Analysis of Timing Jitters in CMOS Ring Oscillators," pp. 27-30.
	Niknejad et al., "Analysis, Design, and Optimization of Spiral Inductors and Transformers for Si RF IC's," October 1998, pp. 1470-1481.
	Gray et al., Analysis and Design of Analog Integrated Circuits, Fourth Edition.
	American National Standard, "Fibre Distributed Data Interface (FDDI) – Token Ring Twisted Pair Layer Medium Dependent (TP-PMD)," September 25, 1995.
	Nguyen et al., "Si IC-Compatible Inductors and LC Passive Filters," August 1990, pp. 1028-1031.
	Gardner, "Charge-Pump Phase-Lock Loops," November 1980, pp. 1849-1858.
	Dally et al., "High Performance Electrical Signaling."
	Davies, "Digital Generation of Low-Frequency Sine Waves," June 1969, pp. 97-105.
	Abidi, "TP 11.1: Direct-Conversion Radio Transceivers for Digital Communications," 1995.
	Dolle, "A Dynamic Line-Termination Circuit for Multireceiver Nets," December 1993, pp. 1370-1373.
	Su et al., "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits," April 1993, pp. 420-430.
	Gray et al., "Future Directions in Silicon ICs for RF Personal Communications," 1995, pp. 83-90.
	Gabara, "On-Chip Terminating Registers for High Speed ECL-CMOS Interfaces," 1992, pp. 292-295.
✓	Horowitz et al., "High-Speed Electrical Signaling: Overview and Limitations," 1998, pp. 12-24.

EXAMINER	P John	DATE CONSIDERED	9/13/05
----------	--------	-----------------	---------

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

14 of 27



FORM PTO 1449 MODIFIED  
U.S. PATENT AND TRADEMARK OFFICE

ATTORNEY DOCKET NO.	APPLICATION NO.
MP0020	09/737,743
APPLICANT	GROUP
Sehat SUTARDJA	2631

### LIST OF REFERENCES CITED BY APPLICANT

DATE SUBMITTED TO USPTO: July 22, 2005

### FOREIGN PATENT DOCUMENTS

*EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION OR ABSTRACT

### OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)

MP	Kim et al., "A 30-MHz Hybrid Analog/Digital Clock Recovery Circuit in 2- $\mu$ m CMOS," 1990, pp. 1385-1394.
	Liu et al., "WP 23.7: A 6.5 GHz Monolithic CMOS Voltage-Controlled Oscillator," 1999, pp. 404-405, 484.
	Wang et al., "WP 23.8: A 9.8 GHz Back-Gate Tuned VCO in 0.35 $\mu$ m CMOS," 1999, pp. 406-407, 484.
	Rofougaran et al., "SP 24.6: A 900 MHz CMOS LC-Oscillator with Quadrature Outputs," 1996.
	Koullias et al., "TP 9.2: A 900 MHz Transceiver Chip Set for Dual-Mode Cellular Radio Mobile Terminals," 1993, pp. 140-141, 278.
	Dauphinee et al., "SP 23.7: A Balanced 1.5 GHz Voltage Controlled Oscillator with an Integrated LC Resonator," 1997, pp. 390-391, 491.
	Banu et al., "A BiCMOS Double-Low-IF Receiver for GSM," 1997, pp. 521-524.
	Chang et al., "A CMOS Channel-Select Filter for a Direct-Conversion Wireless Receiver," 1996, pp. 62-63.
	Waizman, "FA 18.5: A Delay Line Loop for Frequency Synthesis of De-Skewed Clock," February 18, 1994, pp. 298-299.
	Kinget, "FP 14.7: A Fully Integrated 2.7V 0.35 $\mu$ m CMOS VCO for 5 GHz Wireless Applications," February 5, 1998.
	Lee et al., "A Fully Integrated Low-Noise 1-GHz Frequency Synthesizer Design for Mobile Communication Application," May 1997, pp. 760-765.
	Parker et al., "A Low-Noise 1.6-GHz CMOS PLL with On-Chip Loop Filter," 1997, pp. 407, 409-410.
	Park et al., "A Low-Noise, 900-MHz VCO in 0.6 $\mu$ m CMOS," May 1999, pp. 586-591.
	Soyer et al., "A Monolithic 2.3-Gb/s 100-mW Clock and Data Recovery Circuit in Silicon Bipolar Technology," December 1993, pp. 1310-1313.
	Hu et al., "A Monolithic 480 Mb/s Parallel AGC/Decision/Clock-Recovery Circuit in 1.2- $\mu$ m CMOS," December 1993, pp. 1314-1320.
	Parameswaran et al., "A New Approach for the Fabrication of Micromechanical Structures," December 6, 1998, pp. 289-307.
↓	Cho et al., "TP 13.5: A Single-Chip CMOS Direct-Conversion Transceiver for 900 MHz Spread-Spectrum Digital Cordless Phones," 1999, pp. 228-229, 464.

EXAMINER

Pyun

DATE CONSIDERED

9/13/05

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

150827



FORM PTO 1449 MODIFIED  
U.S. PATENT AND TRADEMARK OFFICE

ATTORNEY DOCKET NO.	APPLICATION NO.
MP0020	09/737,743
APPLICANT	
Sehat SUTARDJA	
FILING DATE	GROUP
12/18/2000	2631

## LIST OF REFERENCES CITED BY APPLICANT

DATE SUBMITTED TO USPTO: July 22, 2005

### FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION OR ABSTRACT

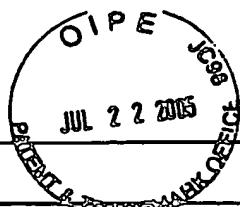
### OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)

✓	Sedra et al., Microelectronic Circuits, Third Edition, 1991, pp. 86-92.
	Moon et al., "An All Analog Multiphase Delay Locked Loop Using a Replica Delay Line for Wide Range Operation and Low-Jitter Performance," March 2000, pp. 377-384.
	I.E.E.E. Standard 802.3: Part 3, "Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Detection," March 8, 2002, pp. 1-378.
	Shoval et al., "WA 18.7 – A Combined 10/125 Mbaud Twisted-Pair Line Driver with Programmable Performance/Power Features," 2000, pp. 314-315.
	Myson Technology, "MTD214 – Ethernet Encoder/Decoder and 10BaseT Transceiver with Built-in Waveform Shaper," 1997, pp. 1-11.
	Myson Technology, "MTD972 (Preliminary) 100BaseTX PCS/PMA," 1997, pp. 1-21.
	Craninckx et al., "A 1.8-GHz Low-Phase-Noise CMOS VCO Using Optimized Hollow Spiral Inductors," 1997, pp. 736-744.
	Craninckx et al., "A 1.8-GHz Low-Phase-Noise CMOS VCO Using Optimized Hollow Spiral Inductors," 1995, pp. 1474-1482.
	Hung et al., "A 1.24-GHz Monolithic CMOS VCO with Phase Noise of 137 dBc/Hz at a 3-MHz Offset," 1999, pp. 111-113.
	Rudell et al., "A 1.9-GHz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications," 1997, pp. 2071-2088.
	Lin et al., "TP 12.5: A 1.4 GHz Differential Low-Noise CMOS Frequency Synthesizer using a Wideband PLL Architecture," 2000, pp. 204-205, 458.
	Razavi, "SP 23.6: A 1.8 GHz CMOS Voltage-Controlled Oscillator," 1997, pp. 388-389.
	Dec et al., "MP 4.8: A 1.9 GHz Micromachine-Based Low-Phase-Noise CMOS VCO," 1999, pp. 80-81, 449.
	Sato et al., "SP 21.2: A 1.9 GHz Single-Chip IF Transceiver for Digital Cordless Phones," February 10, 1996.
	Rudell et al., "SA 18.3: A 1.9 GHz Wide-band IF Double Conversion CMOS Integrated Receiver for Cordless Telephone Applications," 1997, pp. 304-305, 476.
	Lee et al., "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabytes/s DRAM," 1994, pp. 1491-1496.
	Leong et al., "A 2.7-V 900-MHz/1.9-GHz Dual-Band Transceiver IC for Digital Wireless Communication," 1999, pp. 286-291.
	Lam et al., "WP 23.6: A 2.6 GHz/5.2 GHz CMOS Voltage-Controlled Oscillator," 1999, pp. 402-403, 484.
✓	Marshall et al., "TA 8.7: A 2.7V GSM Transceiver ICs with On-Chip Filtering," 1995.

EXAMINER	<i>Dphm</i>	DATE CONSIDERED	<i>9/13/05</i>
----------	-------------	-----------------	----------------

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

*16 of 27*



FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE		ATTORNEY DOCKET NO.	APPLICATION NO.
		MP0020	09/737,743
LIST OF REFERENCES CITED BY APPLICANT		APPLICANT	
		Sehat SUTARDJA	
DATE SUBMITTED TO USPTO: July 22, 2005		FILING DATE	GROUP
		12/18/2000	2631

#### FOREIGN PATENT DOCUMENTS

*EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION OR ABSTRACT
pw	62-159925	7/15/87	JP			
pw	6-276182	9/30/94	JP			

#### OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)

pw	Sedra et al., Microelectronic Circuits, 3rd ed., 1991
	Yee et al., An Integratable 1-2.5 Gbps Low Jitter CMOS Transceiver with Built in Self Test Capability, 1999
	Intersil, HC-5509B ITU CO/Loop Carrier SLIC, 8/2003
	Regan, ADSL Line Driver/Receiver Design Guide, Part 1, 2/2000
	Phillips, The HC-5502X14X Telephone Subscriber Line Interface Circuits (SLIC), 1/1997
	Fuad Et al., An Operational Amplifier Circulator Based on the Weighted Summer, 6/1975
	Narayanan et al., Doppler Estimation Using a Coherent Ultrawide-Band Random Noise Radar, 6/2000
	Stephens, Active Output Impedance for ADLS Line Drivers, 11/2002
	High Speed Modem Solutions Info Card 20
	Hellums et al., An ADSL Integrated Active Hybrid Circuit
	Everitt et al., A CMOS Transceiver for 10-Mb/s and 100-Mb/s Ethernet, 12/1998
	Azadet et al., A Gigabit Transceiver Chip Set for UTP CA-6 Cables in Digital CMOS Technology, 2/2000
	He et al., A DSP Receiver for 1000 Base-T PHY, 2001
	Baird et al., A Mixed Sample 120M s PRML Solution for DVD Systems, 1999
	Baker, An Adaptive Cable Equalizer for Serial Digital Rates to 400Mb/s, 1996
	Chan et al., A 100 Mb/s CMOS 100Base-T4 Fast Ethernet Transceiver for Category 3, 4 & 5 UTP, 1998
	Everitt et al., A 10/100Mb/s CMOS Ethernet Transceiver for 10BaseT, 10BaseTX and 100Base FX, 1998
	Kelly et al., A Mixed Signal DFE/Ffe Receiver for 100BaseTX Applications, 2000
	Shoaei et al., A 3V Low Power 0.25um CMOS 100Mb/s Receiver for Fast Ethernet, 2000
	Walker et al., A Two Chip 1.5 GBd Serial Link Interface, 12/1992
	Linear Technology High Speed Modem Solutions Info Card

EXAMINER	pw	DATE CONSIDERED	9/13/01
----------	----	-----------------	---------

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

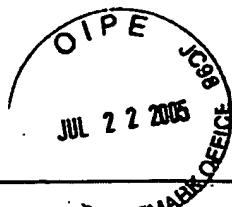
17 of 27



FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE		ATTORNEY DOCKET NO.	APPLICATION NO.
		MP0020	09/737,743
<b>LIST OF REFERENCES CITED BY APPLICANT</b>		APPLICANT	
		Sehat SUTARDJA	
DATE SUBMITTED TO USPTO: July 22, 2005		FILING DATE	GROUP
		12/18/2000	2631
<b>OTHER DOCUMENTS</b> (Including author, title, date, pertinent pages, etc.)			
 	Mueller, Combining Echo Cancellation and Decision Feedback Equalization, 02/29/1979		
	Roo et al., A CMOS Transceiver Analog Front-end for Gigabit Ethernet over Cat-5 Cables, 2001		
	Shoval, A Combined 10/125 Mbaud Twisted Pair Line Driver with Programmable Performance/Power Features, 2000		
	Knight, Jr. et al., A Self-Terminating Low-Voltage Swing CMOS Output Driver, 1988, 457-464		
	Maneatis, Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques, 11/1996, 1723-1732		
	Chang et al., Large Suspended Inductors on Silicon and Their Use in a 1-um CMOS RF Amplifier, 5/1993, 246-248		
	Gharpurey et al., Modeling and Analysis of Substrate Coupling in Integrated Circuits, 3/1996, 344-353		
	Young et al., Monolithic High-Performance three-Dimensional Coil Inductors for Wireless Communications, 1997		
	Efendovich et al., Multifrequency Zero-Jitter Delay-Locked Loop, 1/1994, 67-70		
	Munshi et al., Adaptive Impedance Matching, 69-72		
	Niknejad et al., Numerically Stable Green Function for Modeling and Analysis fo Substrate Coupling in Integrated Circuits, 4/1998, 305-315		
	Hajimiri et al., Phase Noise in Multi-Gigahertz CMOS Ring Oscillators, 1998, 49-52		
	Kim et al., PLL/DLL System Noise Analysis for Low Jitter Clock Synthesizer Design, 31-34		
	Rudell et al., Recent Developments in High Integration Multi-Standard CMOS Transceivers for Personal Communication Systems, 1998, 149-154		
	Shoval et al., A 100 Mb/s BiCMOS Adaptive Pulse-Shaping Filter, 12/1995, 1692-1702		
Jansen et al., SP 23.8: Silicon Bipolar VCO Family for 1.1 to 2.2 GHz with Fully-Integrated Tank and Tuning Circuits, 2/8/1997, 392-393 & 492			
EXAMINER		DATE CONSIDERED	9/13/05

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

18 of 27



FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE		TRADEMARK OFFICE		ATTORNEY DOCKET NO.	APPLICATION NO.		
				MP0020	09/737,743		
LIST OF REFERENCES CITED BY APPLICANT				APPLICANT			
				Sehat SUTARDJA			
DATE SUBMITTED TO USPTO: July 22, 2005				FILING DATE	GROUP		
				12/18/2000	2631		
U.S. PATENT DOCUMENTS							
EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
✓	3,973,089	8/3/1976	Puckett				
	4,131,767	12/26/78	Weinstein				
	4,321,753	3/30/82	Fusari				
	4,535,206	8/13/85	Falconer				
	4,621,356	11/04/1986	Scipione				
	4,715,064	11/22/87	Claessen				
	4,727,566	2/23/88	Dahlqvist				
	4,817,081	3/28/89	Wouda et al.				
	4,878,244	10/31/89	Gawargy, M.				
	4,888,762	12/19/89	Arai				
	4,894,820	1/16/90	Miyamoto				
	4,970,715	11/13/90	McMahan				
	4,993,045	2/12/91	Alfonso				
	5,018,134	5/21/91	Kokubo et al.				
	5,119,365	6/2/92	Warner et al.				
	5,148,427	9/15/92	Buttle et al.				
	5,243,346	9/7/93	Inami				
	5,245,654	9/14/93	Wilkison et al.				
	5,248,956	9/28/93	Himes				
	5,253,249	11/12/93	Fitzgerald et al.				
	5,280,526	1/18/94	Laturell				
	5,282,157	1/25/94	Murphy et al.				
	5,365,935	11/22/94	Righter et al.				
	5,367,540	11/22/94	Kakushi et al.				
✓	5,465,272	11/7/95	Smith				
EXAMINER <i>Phueng Huu</i>		DATE CONSIDERED		9/13/05			

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

19 of 27



FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE				ATTORNEY DOCKET NO.	APPLICATION NO.		
				MP0020	09/737,743		
LIST OF REFERENCES CITED BY APPLICANT				APPLICANT			
				Sehat SUTARDJA			
DATE SUBMITTED TO USPTO: July 22, 2005				FILING DATE	GROUP		
				12/18/2000	2631		
U.S. PATENT DOCUMENTS							
*EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
Py		5,507,036	4/9/96	Vagher			
		5,557,027	11/19/96	Cheng			
		5,613,233	3/18/97	Vagher			
		5,812,597	9/22/98	Graham et al.			
		5,841,809	11/24/98	Koizumi et al.			
		5,887,059	3/23/99	Xie et al.			
		5,894,496	4/13/99	Jones			
		5,930,686	7/27/99	Devline et al.			
		6,005,370	12/21/99	Gustavson			
		6,038,266	3/14/00	Lee et al.			
		6,192,226	2/20/01	Fang			
		6,266,367	7/24/01	Strait			
		6,259,680	7/10/01	Blackwell et al.			
		6,259,957	7/10/01	Alexander et al.			
		6,377,683	4/23/02	Dobson et al.			
		6,389,077	5/14/02	Chan			
		6,408,032	6/18/02	Lye et al.			
		6,163,579	12/19/00	Harrington et al.			
		6,259,680	7/10/01	Blackwell et al.			
		6,731,748	5/4/04	Edgar et al.			
		6,744,831	6/1/04	Chan			
		6,751,202	6/15/04	Henrie			
		2002-0009057	6/24/02	Blackwell et al.			
		2003-0174660	9/18/03	Blon et al.			
		5,651,029	7/22/97	Yang et al.			
EXAMINER <i>phung phu</i>				DATE CONSIDERED <i>9/13/05</i>			

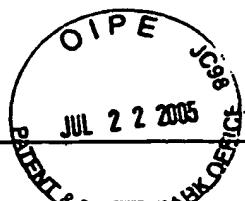
\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

20 of 27



FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE		ATTORNEY DOCKET NO.	APPLICATION NO.				
		MP0020	09/737,743				
LIST OF REFERENCES CITED BY APPLICANT		APPLICANT					
		Sehat SUTARDJA					
DATE SUBMITTED TO USPTO: July 22, 2005		FILING DATE	GROUP				
		12/18/2000	2631				
U.S. PATENT DOCUMENTS							
*EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
V	6,173,019	1/9/01	Hee et al.				
	6,223,061	4/24/01	Dacus et al.				
	6,236,645	5/22/01	Agazzi				
	6,259,957	7/10/01	Alexander et al.				
	6,298,046	10/2/01	Thiele				
	6,421,534	7/16/02	Cook et al.				
	6,823,028	11/23/04	Phanse				
	6,043,766	3/28/00	Hee et al.				
	6,044,489	3/29/00	Hee et al.				
	5,269,313	12/14/93	DiPinto				
	5,880,615	3/9/99	Bazes				
	6,140,857	10/31/00	Bazes				
	6,148,025	11/14/00	Shirani et al.				
	6,211,716	4/3/01	Nguyen et al.				
	6,385,238	5/7/02	Nguyen et al.				
	6,408,032	6/18/02	Lye et al.				
	6,415,003	7/2/02	Raghaven				
	4,621,172	11/04/86	Kanemasa et al.				
	6,370,190	4/9/02	Young et al.				
	6,201,831	3/13/01	Agazzi et al.				
	6,377,640	4/23/02	Trans				
	5,579,004	11/26/96	Linz				
	5,577,027	11/19/96	Cheng				
	5,365,935	11/22/94	Righter et al.				
	6,049,706	4/11/00	Cook et al.				
V	6,731,748	5/4/04	Edgar, III et al.				
EXAMINER <i>Phung phuc</i>		DATE CONSIDERED <i>9/13/05</i>					

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



**EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

22 of 27



FORM PTO 1449 MODIFIED  
U.S. PATENT AND TRADEMARK OFFICE

ATTORNEY DOCKET NO.	APPLICATION NO.
MP0020	09/737,743

### LIST OF REFERENCES CITED BY APPLICANT

DATE SUBMITTED TO USPTO: July 22, 2005

APPLICANT
Sehat SUTARDJA

FILING DATE	GROUP
12/18/2000	2631

### U.S. PATENT DOCUMENTS

*EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
W	6,163,579	12/19/2000	Harrington et al.			
	4,621,172	11/04/1986	Kanemasa et al.			
	5,841,809	11/24/1988	Koizumi et al.			
	5,018,134	05/21/1991	Kobuku et al.			
	5,280,526	01/18/1994	Laturell			
	4,970,715	11/13/1990	McMahon			
	5,282,157	01/25/1994	Murphy et al.			
	4,131,767	12/26/1978	Weinstein			
	5,245,654	09/14/1993	Wilkison et al.			
	4,817,081	03/28/1989	Wouda et al.			
	5,887,059	03/23/1999	Xie et al.			
	6,462,688	10/08/2002	Sutardja			
	3,543,009	11/24/1970	Voelcker			
	3,297,951	01/10/1967	Blasbalg			
	4,071,842	01/31/1978	Tewksbury			
	4,309,673	01/05/1982	Norberg et al.			
	4,408,190	10/04/1983	Nagano			
	4,464,545	08/07/1984	Werner			
	5,403,421	03/05/1985	Hareyama			
	4,527,126	07/02/1985	Petricich et al.			
	4,591,832	05/27/1986	Fling et al.			
	4,605,826	08/12/1986	Kanemasa			
	4,626,803	12/02/1986	Holm			
	4,816,830	03/28/1989	Cooper			
V	4,868,571	09/19/1989	Inamasu			

EXAMINER

phuong phu

DATE CONSIDERED

1/13/05

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

23 of 27



FORM PTO 1449 MODIFIED  
U.S. PATENT AND TRADEMARK OFFICE

**LIST OF REFERENCES CITED BY APPLICANT**

DATE SUBMITTED TO USPTO: July 22, 2005

ATTORNEY DOCKET NO.	APPLICATION NO.
MP0020	09/737,743
APPLICANT	
Sehat SUTARDJA	
FILING DATE	GROUP
12/18/2000	2631

**U.S. PATENT DOCUMENTS**

*EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
PP	4,972,360	11/20/1990	Cukier et al.			
	4,988,960	01/29/1991	Tomisawa			
	5,084,865	01/28/1992	Koike			
	5,136,260	08/04/1992	Yousefi-Elezei			
	5,212,659	05/18/1993	Scott et al.			
	5,245,231	09/14/1993	Kocis et al.			
	5,253,272	10/12/1993	Jaeger et al.			
	5,307,064	04/26/1994	Kudoh			
	5,307,405	04/26/1994	Sih			
	5,323,157	06/21/1994	Ledzius et al.			
	5,357,145	10/18/1994	Segaram			
	5,375,147	12/20/1994	Awata et al.			
	5,388,123	02/07/1995	Uesugi et al.			
	5,392,042	02/21/1995	Pellon			
	5,444,739	08/22/1995	Uesegi et al.			
	5,517,435	05/14/1996	Sugiyama			
	5,537,113	07/16/1996	Kawabata			
	5,539,403	07/23/1996	Tani et al.			
	5,539,773	07/23/1996	Knee et al.			
	5,568,142	10/22/1996	Velazquez et al.			
	5,579,004	11/26/1996	Linz			
	5,651,029	07/22/1997	Yang et al.			
	5,659,609	08/19/1997	Koizumi et al.			
	5,684,482	11/04/1997	Galton			
↓	5,696,796	12/09/1997	Poklemba			

EXAMINER

Phumy plm

DATE CONSIDERED

9/13/05

24 of 27

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



FORM PTO 1449 MODIFIED  
U.S. PATENT AND TRADEMARK OFFICE

### LIST OF REFERENCES CITED BY APPLICANT

DATE SUBMITTED TO USPTO: July 22, 2005

ATTORNEY DOCKET NO.	APPLICATION NO.
MP0020	09/737,743
APPLICANT	
Sehat SUTARDJA	
FILING DATE	GROUP
12/18/2000	2631

### U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
W	5,963,069	10/05/1999	Jefferson et al.			
	5,982,317	11/09/1999	Steensgaard-Madsen			
	6,014,048	01/11/2000	Talaga et al.			
	6,037,812	03/14/2000	Gaudet			
	6,047,346	04/04/2000	Lau et al.			
	6,067,327	05/23/2000	Creigh et al.			
	6,094,082	07/25/2000	Gaudet			
	6,100,830	08/08/2000	Dedic			
	6,137,328	11/24/2000	Sung			
	6,150,856	11/21/2000	Morzano			
	6,172,634 B1	01/09/2001	Leonowich et al.			
	6,201,490 B1	03/13/2001	Kawano et al.			
	6,215,429 B1	04/10/2001	Fischer et al.			
	6,236,345 B1	05/22/2001	Dagnachew et al.			
	6,249,249 B1	06/19/2001	Obayashi et al.			
	6,259,745 B1	07/10/2001	Chan			
	6,271,782 B1	08/07/2001	Steensgaard-Madsen			
	6,289,068 B1	09/11/2001	Hassoun et al.			
	6,313,775 B1	11/06/2001	Lindfors et al.			
	6,333,959 B1	12/25/2001	Lai et al.			
	6,339,390 B1	01/15/2002	Velazquez et al.			
	6,340,940 B1	01/22/2002	Melanson			
	6,351,229 B1	02/26/2002	Wang			
	6,373,417 B1	04/16/2002	Melanson			
V	6,385,442 B1	05/07/2002	Vu et al.			

EXAMINER

Phu Nguyen

DATE CONSIDERED

9/13/05

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

25 of 27

JUL 22 2005

PARENT &amp; TRADEMARK RECEIVED

FORM PTO 1449 MODIFIED  
U.S. PATENT AND TRADEMARK OFFICE

ATTORNEY DOCKET NO.	APPLICATION NO.
MP0020	09/737,743
APPLICANT	
Sehat SUTARDJA	
FILING DATE	GROUP
12/18/2000	2631

## LIST OF REFERENCES CITED BY APPLICANT

DATE SUBMITTED TO USPTO: July 22, 2005

## U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
✓	6,421,377 B1	07/16/2002	Langberg et al.			
	6,441,761 B1	08/27/2002	Viswanathan			
	6,476,749 B1	11/05/2002	Yeap et al.			
	6,492,922 B1	12/10/2002	New			
	6,509,857 B1	01/21/2003	Nakao			
	6,531,973 B2	03/11/2003	Brooks et al.			
	6,539,072 B1	03/25/2003	Donnelly et al.			
	6,570,931 B1	05/27/2003	Song			
	6,714,825 B1	03/30/2004	Tanaka			
	6,816,097 B2	11/09/2004	Brooks et al.			
	6,844,837 B1	01/18/2005	Sutardja et al.			
	2002-0061087 A1	05/23/2002	Williams			
	2002-0084857 A1	07/04/2002	Kim			
	2004-0141569 A1	07/22/2004	Agazzi			
	5,243,346	09/07/1993	Inami			
	5,267,269	11/30/1993	Shih et al.			
	6,154,784	11/28/2000	Liu			
	6,163,283	12/19/2000	Schofield			
	6,163,289	12/19/2000	Ginetti			
	6,185,263 B1	02/06/2001	Chan			
	6,191,719 B1	02/20/2001	Bult et al.			
	6,249,164 B1	06/19/2001	Cranford Jr. et al.			
	6,259,745 B1	07/10/2001	Chan			
	6,259,012 B1	09/25/2001	Greig			
✓	6,037,490 B1	10/23/2001	Litfin et al.			

EXAMINER

Phuong Phan

DATE CONSIDERED

9/13/05

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

26 of 27



**EXAMINED:** In the following circumstances, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

27 of 27



FORM PTO 1449 MODIFIED  
U.S. PATENT AND TRADEMARK OFFICE

ATTORNEY DOCKET NO.	APPLICATION NO.
MP0020	09/737,743
APPLICANT	
Sehat SUTARDJA	
FILING DATE	GROUP
12/18/2000	2631

### LIST OF REFERENCES CITED BY APPLICANT

DATE SUBMITTED TO USPTO: July 25, 2005

### FOREIGN PATENT DOCUMENTS

*EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION OR ABSTRACT

### OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)

✓	LIBERALI ET AL., "Progress in High-Speed and High -Resolution CMOS Data Converters", September 12-14, 1995, pages 19-28
✓	SEDRA et al., "Micro-Electronic Circuits", 1982, pages 95-97 and 243-247
✓	DP83220 CDL™ Twisted Pair FDDI Transceiver Device", October 1992
✓	SU ET AL., "A CMOS Oversampling D/A Converter with a Current-Mode Semidigital Reconstruction Filter", December 1993, pages 1224-1233
✓	GOLDBERG, Gigabit Ethernet PHY Chip Sets LAN Speed Record for Copper Story" 6 pages
✓	MIKI ET AL., "An 80-MHz 8-bit CMOS D/A Converter", December 1986, pages 983-988
✓	LETHAM ET AL., "A high-performance CMOS 70-Mhzpalette/DAC", December 1987, pages 1041-1047
✓	NAKAMURA ET AL., "A 10-b 70-MS/s CMOS D/A converter", April 1991, pages 637-642
✓	TAKAKURA ET AL., "A10 bit 80 MHz glitchless CMOS D/A converter", May 1991, pages 26.5.1-26.5.4
✓	FOURNIER ET AL., "A 130-MHz 8-b CMOS video DAC for HDTV applications", July 1991, pages 1073-1077
✓	REYNOLDS, "A 320 MHz CMOS triple 8b DAC with on-chip PLL and hardware cursor", February 1994, pages 50-51
✓	CHIN ET AL., "A 10-b 125 MHz CMOS digital-to-analog (DAC) with threshold-voltage compensated current sources", November 1994, pages 1374-1380
✓	WU ET AL., "A low glitch 10-bit 75-MHz CMOS video D/A converter, January 1995, pages 68-72
✓	The Authoritative Dictionary of IEEE Standards Stems 7th Edition, page 280
✓	GRAY ET AL., "Analysis and Design of Analog Integrated Circuits, 1997

EXAMINER

*Pyhun*

DATE CONSIDERED

*7/13/05*

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE		ATTORNEY DOCKET NO.		APPLICATION NO.	
		MP0020		09/737,743	
<b>LIST OF REFERENCES CITED BY APPLICANT</b>		APPLICANT			
		Sehat SUTARDJA			
DATE SUBMITTED TO USPTO: July 25, 2005		FILING DATE		GROUP	
		12/18/2000		2631	
<b>U.S. PATENT DOCUMENTS</b>					
*EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS
MP	5,254,994	10/19/1993	Takakura et al.		
	5,585,802	12/17/1996	Cabler et al.		
	5,821,892	10/13/1998	Smith		
	3,500,215	03/10/1970	Leuthold et al.		
	3,521,170	11/27/1970	Leuthold et al.		
	3,793,589	02/19/1974	Puckette		
	4,393,370	07/12/1993	Hareyama		
	6,476,476 B2	11/05/2002	Viswanathan		
	4,947,171	08/07/1990	Pfeifer		
	6,309,077 B1	10/30/2001	Saif et al.		
	6,594,304 B2	07/15/2003	Chan		
	6,411,647 B1	06/25/2002	Chan		
	6,744,931 B2	06/01/2004	Komiya et al.		
	6,373,908 B2	04/16/2002	Chan		
	5,153,450	10/06/1992	Ruetz		
	5,572,159	11/05/1996	McFarland		
	6,535,987 B1	03/18/2003	Ferrant		
↓	6,633,178 B2	10/14/2003	Wilcox et al.		
EXAMINER		DATE CONSIDERED		9/13/05	

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE				ATTORNEY DOCKET NO.	APPLICATION NO.		
				MP0020	09/737,743		
LIST OF REFERENCES CITED BY APPLICANT				APPLICANT			
				Sehat SUTARDJA			
DATE SUBMITTED TO USPTO: July 29, 2005				FILING DATE	GROUP		
				12/18/2000	2631		
FOREIGN PATENT DOCUMENTS							
*EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION OR ABSTRACT	
W	06-97831	04/08/1994	Japan			with Translation	
	05-064231 A	03/12/1993	Japan			Abstract	
	09-55770	08/17/1995	Japan			with Translation	
	09-270707	03/03/1996	Japan			with Translation	
✓	2001-177409	12/16/1999	Japan			with Translation	
OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)							
W	Hellwarth, et al., "Digital-to-analog Converter having Common-mode Isolation and Differential Output".						
	Sedra et al., Microelectronic Circuits, Third Edition, 1991, pp. 48-115.						
	Lee, et al., " A CMOS Serial Link for Fully Duplexed Data Communication", April, 1995.						
	Shoval et al., "WA 18.7 – A Combined 10/125 Mbaud Twisted-Pair Line Driver with Programmable Performance/Power Features," 2000, pp. 314-315.						
	Song, et al., "FP 12.1: NRZ Timing Recovery Technique for Band-Limited Channels (Slide Supplement), 1996.						
	Chien, "Monolithic CMOS Frequency Synthesizer for Cellular Applications", March 12-13.						
	Chien, "Delay Based Monolithic CMOS Frequency Synthesizer for Portable Wireless Applications", May 20, 1998.						
	Chien, "Low-Noise Local Oscillator Design Techniques using DLL-based Frequency Multiplier for Wireless Applications", 2000.						
	Cho et al.; "A Single-Chip CMOS Direct Conversion Transceiver for 900 MHz Spread-Spectrum Digital Cordless Telephones"; 1999						
	Shoval et al.; "A CMOS Mixed-Signal 100Mb/s Receive Architecture for Fast Ethernet"; 1999						
	Hester et al.; "CODEC for Echo-Canceling Full-Rate ADSL Modems"; December, 1999						
	Nack, et al., "A Constant Slew Rate Ethernet Line Driver", May, 2001.						
	Song, "Dual Mode Transmitter with Adaptively Controlled Slew Rate and Impedance Supporting Wide Range Data Rates", 2001.						
	Yee et al., An Integratable 1-2.5 Gbps Low Jitter CMOS Transceiver with Built in Self Test Capability, 1999						
	Intersil, HC-5509B ITU CO/Loop Carrier SLIC, 8/2003						
	Regan, ADSL Line Driver/Receiver Design Guide, Part 1, 2/2000						
	Phillips, The HC-5502X14X Telephone Subscriber Line Interface Circuits (SLIC), 1/1997						
✓	Fuad Surial Atiya, et al., An Operational Amplifier Circulator Based on the Weighted Summer, 6/1975						
EXAMINER		DATE CONSIDERED		9/13/05			
<small>* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</small>							

FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE		ATTORNEY DOCKET NO.	APPLICATION NO.
		MP0020	09/737,743
<b>LIST OF REFERENCES CITED BY APPLICANT</b>		APPLICANT	
		Sehat SUTARDJA	
DATE SUBMITTED TO USPTO: July 29, 2005		FILING DATE	GROUP
		12/18/2000	2631
<b>OTHER DOCUMENTS</b>			
<p>✓ Narayanan et al., Doppler Estimation Using a Coherent Ultrawide-Band Random Noise Radar, 6/2000</p> <p>✓ Stephens, Active Output Impedance for ADLS Line Drivers, 11/2002</p> <p>✓ Hellums et al., An ADSL Integrated Active Hybrid Circuit</p> <p>✓ Azadet et al., A Gigabit Transceiver Chip Set for UTP CA-6 Cables in Digital CMOS Technology, 2/2000</p> <p>✓ He et al., A DSP Receiver for 1000 Base-T PHY, 2001</p> <p>✓ Baird et al., A Mixed Sample 120M s PRML Solution for DVD Systems, 1999</p> <p>✓ Baker, An Adaptive Cable Equalizer for Serial Digital Rates to 400Mb/s, 1996</p> <p>✓ Everitt et al., A 10/100Mb/s CMOS Ethernet Transceiver for 10BaseT, 10BaseTX and 100Base FX, 1998</p> <p>✓ Roo et al., A CMOS Transceiver Analog Front-end for Gigabit Ethernet over Cat-5 Cables, 2001</p> <p>✓ Shoaei et al., A 3V Low Power 0.25um CMOS 100Mb/s Receiver for Fast Ethernet, 2000</p> <p>✓ Walker et al., A Two Chip 1.5 GBd Serial Link Interface, 12/1992</p> <p>✓ Chien, et al., "TP 12.4: A 900-MHz Local Oscillator using a DLL-based Frequency Multiplier Technique for PCS Applications".</p> <p>✓ Lee, et al., "A 3V 10b 100 MS/s Digital-to-Analog Converter for Cable Modem Applications, August 28-30, 2000 pp. 203-205.</p> <p>✓ Rudell, et al., "SA 18.3: A 1.9 GHz Wide-band IF Double Conversion CMOS Integrated Receiver for Cordless Telephone Applications," 1997, pp. 304-305, 476.</p> <p>✓ Young, et al., "Monolithic High-Performance three-Dimensional Coil Inductors for Wireless Communications, 1997</p> <p>✓ Wu, et al., "A low glitch 10-bit 75 MHz CMOS video D/A converter, January 1995, pp. 68-72</p>			
EXAMINER		DATE CONSIDERED	
<p><i>bym</i> 9/13/05</p> <p>* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>			

FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE		ATTORNEY DOCKET NO.	APPLICATION NO.
		MP0020	09/737,743
LIST OF REFERENCES CITED BY APPLICANT		APPLICANT	
		Sehat SUTARDJA	
DATE SUBMITTED TO USPTO: July 29, 2005		FILING DATE	GROUP
		12/18/2000 2631	

#### FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION OR ABSTRACT
plm	63-300700	07/12/1988	Japan			Abstract
	06-029853	02/04/1994	Japan			Abstract
	62-159925	7/15/87	Japan			with Translation
↓	6-276182	9/30/94	Japan			with Translation

#### OTHER DOCUMENTS (including author, title, date, pertinent pages, etc.)

plm	Johns, et al., "Integrated Circuits for Data Transmission Over Twisted Pair Channels", March, 1997, pgs. 398-406.
	"IEEE Standard 802.3: Part 3 Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Detection", March 8, 2002, pages 1-1538
	Young, et al., "A Low-Noise RF Voltage-Controlled Oscillator Using On-Chip High-Q Three-Dimensional Coil Inductor and Micromachined Variable Capacitor", June 8-11, 1998, pgs. 128-131.
	Young, et al., "A Micromachined Variable Capacitor for Monolithic Low-Noise VCOS", 1996, pgs. 86-89.
	Abidi, et al., "FA 7.2: The Future of CMOS Wireless Transceivers", February 7, 1997, pgs. 118-119, 440.
	Eto, et al., "A 333 MHz, 20mW, 18ps Resolution Digital DLL using Current-controlled Delay with Parallel Variables Resistor DAC (PVR-DAC)", August 28-30, 2000, pgs. 349-350.
	Ivan Jorgensen, et al., "Design of a 10-bit 100 MSamples/s BiCMOS D/A Converter", 1996, pgs. 730-733.
	Henriques, et al., "A CMOS Steering-Current Multiplying Digital-to-Analog Converter", 1995, pgs. 145-155.
	Wikner, et al., "Modeling of CMOS Digital-to-Analog Converters for Telecommunication", May, 1999, pgs. 489-499.
	Van der Plas, et al., "A 14-Bit Intrinsic Accuracy Q <sup>2</sup> Random Walk CMOS DAC", December, 1999, pgs. 1708-1718.
	Radke, et al., "A 14-Bit Current-Mode ΣΔ DAC Based Upon Rotated Data Weighted Averaging", August, 2000, pgs. 1074-1084.
	Shui, et al., "Mismatch Shaping for a Current-Mode Multibit Delta-Sigma DAC", March, 1999, pgs. 331-338.
	Hamasaki, et al., "A 3-V, 22-mV Multibit Current-Mode ΣΔ DAC with 100 dB Dynamic Range", December, 1996, pgs. 1888-1894.
	Van de Plassche, "Integrated Analog-to-Digital and Digital-to-Analog Converters – Chapter 6, pgs. 211-271.
	Millman, et al., "Pulse, Digital, and Switching Waveforms", pgs. 674-675.
↓	Tsutomu Kamoto, "An 8-bit 2-ns Monolithic DAC", February, 1988.

EXAMINER	plm	DATE CONSIDERED	9/13/01
----------	-----	-----------------	---------

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

**LIST OF REFERENCES CITED BY APPLICANT**

DATE SUBMITTED TO USPTO: July 29, 2005

FILING DATE **GROUP**  
12/18/2000 **2631****FOREIGN PATENT DOCUMENTS**

*EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION OR ABSTRACT

**OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)**

✓	Weaver, Jr., "A Third Method of Generation and Detection of Single-Sideband Signals," December 1956, pp. 1703-1705.
	Niknejad et al., "Analysis and Optimization of Monolithic Inductors and Transformers for RF ICs," 1997, pp. 375-378.
	Weigandt et al., "Analysis of Timing Jitters in CMOS Ring Oscillators," pp. 27-30.
	Niknejad et al., "Analysis, Design, and Optimization of Spiral Inductors and Transformers for Si RF IC's," October 1998, pp. 1470-1481.
	American National Standard, "Fibre Distributed Data Interface (FDDI) – Token Ring Twisted Pair Layer Medium Dependent (TP-PMD)," September 25, 1995.
	Nguyen et al., "Si IC-Compatible Inductors and LC Passive Filters," August 1990, pp. 1028-1031.
	Gardner, "Charge-Pump Phase-Lock Loops," November 1980, pp. 1849-1858.
	Dally et al., "High Performance Electrical Signaling."
	Davies, "Digital Generation of Low-Frequency Sine Waves," June 1969, pp. 97-105.
	Abidi, "TP 11.1: Direct-Conversion Radio Transceivers for Digital Communications," 1995.
	Dolle, "A Dynamic Line-Termination Circuit for Multireceiver Nets," December 1993, pp. 1370-1373.
	Su et al., "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits," April 1993, pp. 420-430.
	Gray et al., "Future Directions in Silicon ICs for RF Personal Communications," 1995, pp. 83-90.
	Gabara, "On-Chip Terminating Registers for High Speed ECL-CMOS Interfaces," 1992, pp. 292-295.
	Horowitz et al., "High-Speed Electrical Signaling: Overview and Limitations," 1998, pp. 12-24.
	Efendovich et al., Multifrequency Zero-Jitter Delay-Locked Loop, 1/1994, 67-70
	Munshi et al., Adaptive Impedance Matching, 69-72
	Niknejad et al., Numerically Stable Green Function for Modeling and Analysis of Substrate Coupling in Integrated Circuits, 4/1998, 305-315
	Hajimiri et al., Phase Noise in Multi-Gigahertz CMOS Ring Oscillators, 1998, 49-52
✓	Kim et al., PLL/DLL System Noise Analysis for Low Jitter Clock Synthesizer Design, 31-34

EXAMINER

yjmln

DATE CONSIDERED

7/13/08

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ATTORNEY DOCKET NO. **MP0020** APPLICATION NO. **09/737,743****LIST OF REFERENCES CITED BY APPLICANT**

DATE SUBMITTED TO USPTO: July 29, 2005

APPLICANT  
**Sehat SUTARDJA**FILING DATE **12/18/2000** GROUP **2631****FOREIGN PATENT DOCUMENTS**

*EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION OR ABSTRACT

**OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)**

✓	Kim et al., "A 30-MHz Hybrid Analog/Digital Clock Recovery Circuit in 2- $\mu$ m CMOS," 1990, pp. 1385-1394.
	Liu et al., "WP 23.7: A 6.5 GHz Monolithic CMOS Voltage-Controlled Oscillator," 1999, pp. 404-405, 484.
	Wang et al., "WP 23.8: A 9.8 GHz Back-Gate Tuned VCO in 0.35 $\mu$ m CMOS," 1999, pp. 406-407, 484.
	Rofougaran et al., "SP 24.6: A 900 MHz CMOS LC-Oscillator with Quadrature Outputs," 1996.
	Koullias et al., "TP 9.2: A 900 MHz Transceiver Chip Set for Dual-Mode Cellular Radio Mobile Terminals," 1993, pp. 140-141, 278.
	Dauphinee et al., "SP 23.7: A Balanced 1.5 GHz Voltage Controlled Oscillator with an Integrated LC Resonator," 1997, pp. 390-391, 491.
	Banu et al., "A BiCMOS Double-Low-IF Receiver for GSM," 1997, pp. 521-524.
	Chang et al., "A CMOS Channel-Select Filter for a Direct-Conversion Wireless Receiver," 1996, pp. 62-63.
	Waizman, "FA 18.5: A Delay Line Loop for Frequency Synthesis of De-Skewed Clock," February 18, 1994, pp. 298-299.
	Kinget, "FP 14.7: A Fully Integrated 2.7V 0.35 $\mu$ m CMOS VCO for 5 GHz Wireless Applications," February 5, 1998.
	Lee et al., "A Fully Integrated Low-Noise 1-GHz Frequency Synthesizer Design for Mobile Communication Application," May 1997, pp. 760-765.
	Parker et al., "A Low-Noise 1.6-GHz CMOS PLL with On-Chip Loop Filter," 1997, pp. 407, 409-410.
	Park et al., "A Low-Noise, 900-MHz VCO in 0.6 $\mu$ m CMOS," May 1999, pp. 586-591.
	Soyer et al., "A Monolithic 2.3-Gb/s 100-mW Clock and Data Recovery Circuit in Silicon Bipolar Technology," December 1993, pp. 1310-1313.
	Hu et al., "A Monolithic 480 Mb/s Parallel AGC/Decision/Clock-Recovery Circuit in 1.2- $\mu$ m CMOS," December 1993, pp. 1314-1320.
	Parameswaran et al., "A New Approach for the Fabrication of Micromechanical Structures," December 6, 1998, pp. 289-307.
	Knight, Jr. et al., A Self-Terminating Low-Voltage Swing CMOS Output Driver, 1988, 457-464
	Maneatis, Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques, 11/1996, 1723-1732
✓	Chang et al., Large Suspended Inductors on Silicon and Their Use in a 1- $\mu$ m CMOS RF Amplifier, 5/1993, 246-248
✓	Gharpurey et al., Modeling and Analysis of Substrate Coupling in Integrated Circuits, 3/1996, 344-353

EXAMINER

pjlm

DATE CONSIDERED

9/13/01

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ATTORNEY DOCKET NO. **MP0020** APPLICATION NO. **09/737,743****LIST OF REFERENCES CITED BY APPLICANT**

DATE SUBMITTED TO USPTO: July 29, 2005

APPLICANT

Sehat SUTARDJA

FILING DATE **12/18/2000**GROUP **2631****FOREIGN PATENT DOCUMENTS**

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION OR ABSTRACT

**OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)**

W	Shoval et al., "WA 18.7 – A Combined 10/125 Mbaud Twisted-Pair Line Driver with Programmable Performance/Power Features," 2000, pp. 314-315.
	Myson Technology, "MTD214 – Ethernet Encoder/Decoder and 10BaseT Transceiver with Built-in Waveform Shaper," 1997, pp. 1-11.
	Myson Technology, "MTD972 (Preliminary) 100BaseTX PCS/PMA," 1997, pp. 1-21.
	Craninckx et al., "A 1.8-GHz Low-Phase-Noise CMOS VCO Using Optimized Hollow Spiral Inductors," 1997, pp. 736-744.
	Craninckx et al., "A 1.8-GHz Low-Phase-Noise Voltage-Controlled Oscillator with Prescaler," 1995, pp. 1474-1482.
	Hung et al., "A 1.24-GHz Monolithic CMOS VCO with Phase Noise of 137 dBc/Hz at a 3-MHz Offset," 1999, pp. 111-113.
	Rudell et al., "A 1.9-GHz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications," 1997, pp. 2071-2088.
	Lin et al., "TP 12.5: A 1.4 GHz Differential Low-Noise CMOS Frequency Synthesizer using a Wideband PLL Architecture," 2000, pp. 204-205, 458.
	Razavi, "SP 23.6: A 1.8 GHz CMOS Voltage-Controlled Oscillator," 1997, pp. 388-389.
	Dec et al., "MP 4.8: A 1.9 GHz Micromachine-Based Low-Phase-Noise CMOS VCO," 1999, pp. 80-81, 449.
	Sato et al., "SP 21.2: A 1.9 GHz Single-Chip IF Transceiver for Digital Cordless Phones," February 10, 1996.
	Lee et al., "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabytes/s DRAM," 1994, pp. 1491-1496.
	Joo Leong Tham, et al., "A 2.7-V 900-MHz/1.9-GHz Dual-Band Transceiver IC for Digital Wireless Communication," 1999, pp. 286-291.
	Lam et al., "WP 23.6: A 2.6 GHz/5.2 GHz CMOS Voltage-Controlled Oscillator," 1999, pp. 402-403, 484.
✓	Marshall et al., "TA 8.7: A 2.7V GSM Transceiver ICs with On-Chip Filtering," 1995.

EXAMINER

phar

DATE CONSIDERED

7/13/01

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 600; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE		ATTORNEY DOCKET NO.	APPLICATION NO.
		MP0020	09/737,743
LIST OF REFERENCES CITED BY APPLICANT		APPLICANT	
		Sehat SUTARDJA	
DATE SUBMITTED TO USPTO: July 29, 2005		FILING DATE	GROUP
		12/18/2000	2631
OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)			
✓	Rudell et al., Recent Developments in High Integration Multi-Standard CMOS Transceivers for Personal Communication Systems, 1998, 149-154		
	Shoval et al., A 100 Mb/s BiCMOS Adaptive Pulse-Shaping Filter, 12/1995, 1692-1702		
	Jansen et al., SP 23.8: Silicon Bipolar VCO Family for 1.1 to 2.2 GHz with Fully-Integrated Tank and Tuning Circuits, 2/8/1997, 392-393 & 492		
	Cho et al.; "A Single-Chip CMOS Direct Conversion Transceiver for 900 MHz Spread-Spectrum Digital Cordless Telephones"; 1999		
	LIBERALI ET AL., "Progress in High-Speed and High -Resolution CMOS Data Converters", September 12-14, 1995, pages 19-28		
	SEDRA et al., "Micro-Electronic Circuits", 1982, pages 95-97 and 243-247		
	DP83220 CDL™ Twisted Pair FDDI Transceiver Device", October 1992		
	MIKI ET AL., "An 80-MHz 8-bit CMOS D/A Converter", December 1986, pages 983-988		
	LETHAM ET AL., "A high-performance CMOS 70-Mhzpalette/DAC", December 1987, pages 1041-1047		
	NAKAMURA ET AL., "A 10-b 70-MS/s CMOS D/A converter", April 1991, pages 637-642		
	TAKAKURA ET AL., "A10 bit 80 MHz glitchless CMOS D/A converter", May 1991, pages 26.5.1-26.5.4		
	FOURNIER ET AL., "A 130-MHz 8-b CMOS video DAC for HDTV applications", July 1991, pages 1073-1077		
	REYNOLDS, "A 320 MHz CMOS triple 8b DAC with on-chip PLL and hardware cursor", February 1994, pages 50-51		
•	CHIN ET AL., "A 10-b 125 MHz CMOS digital-to-analog (DAC) with threshold-voltage compensated current sources", November 1994, pages 1374-1380		
	The Authoritative Dictionary of IEEE Standards Stems 7th Edition, page 280		
	Chan, et al., "A 100 Mb/s CMOS 100Base-T3 Fast Ethernet Transceiver for Category 3, 4, & 5 UTP, 1998		
✓	WANG, et al., "A 1.2 GHz programmable DLL-Based Frequency Multiplier for Wireless Applications, December 2004		
EXAMINER <i>M. Lue</i>		DATE CONSIDERED	9/13/05
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			



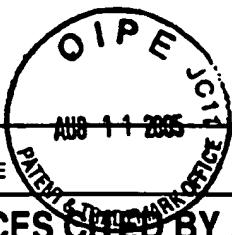




FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE		AUG 09 2005		ATTORNEY DOCKET NO.	APPLICATION NO.		
				MP0020	09/737,743		
LIST OF REFERENCES CITED BY APPLICANT				APPLICANT			
				Sehat SUTARDJA			
DATE SUBMITTED TO USPTO: August 9, 2005				FILING DATE	GROUP		
				12/18/2000	2631		
FOREIGN PATENT DOCUMENTS							
*EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION OR ABSTRACT	
W	WO 00/28663 A3	05/18/2000	Europe				
W	WO 00/28691 A3	05/18/2000	Europe				
OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)							
	Rao, Short Course: Local Area Networks						
	Razavi, Principles of Data Conversion System Design						
	Mano, Digital Logic and Computer Design						
	Farjad-rad, et al., 4.5 A 0.2-2GHz 12mW Multiplying DLL for Low-Jitter Clock Synthesis in Highly Integrated Data Communication Chip						
	Gotoh, et al., All-Digital Multi-Phase Delay Locked Loop for Internal Timing Generation in Embedded and/or High-Speed DRAMS						
	Johnson, et al., THAM 11.2: A Variable Delay Line Phase Locked Loop for CPU-Coprocessor Synchronization						
	Sonntag, et al., FAM: 11.5: A Monolithic CMOS 10MHz DPLL for Burse-Mode						
	Garlepp, et al., A Portable Digital DLL Architecture for CMOS Interface Circuits						
	Lin, et al., A Register-Controller Symmetrical DLL for Double-Data-Rate DRAM						
	Garlepp, et al., A Portable Digital DLL for High-Speed CMOS Interface Circuits						
	Dehng, et al., Clock-Deskaw Buffer Using a SAR-Controlled Delay-Locked Loop						
	Kim, et al., A Low-Power Small-Area 7.28-ps-Jitter 1-GHz DLL-Based Clock Generator						
	Dehng, et al., A Fast-Lock Mixed-Mode DLL Using a 2-b SAR Algorithm						
✓	Lin, et al., A 10-b, 500-Msample/s CMOS DAC in 0.6mm2						
EXAMINER	pmlm		DATE CONSIDERED		9/13/05		
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							



A circular postmark from the U.S. Patent and Trademark Office, Washington, D.C. The text "U.S. PATENT & TRADEMARK OFFICE" is curved along the bottom edge, and "WASHINGTON, D.C." is curved along the top edge. The date "AUG 10 2005" is in the center, with "U.S.P.T.O." written vertically to the left of the date.



**FORM PTO 1449 MODIFIED  
U.S. PATENT AND TRADEMARK OFFICE**

008-11-2885

**ATTORNEY DOCKET NO.**

**APPLICATION NO.**

MP0020

09/737.743

**APPLICANT**

Sehat SUTARDJA

## ~~LIST OF REFERENCES CHECKED BY APPLICANT~~

**DATE SUBMITTED TO USPTO:** August 11, 2005

**FILING DATE**

---

**GROUP**

12/18/2000

2631

## **U.S. PATENT DOCUMENTS**

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
PP	6,462,688	10-08-02	SUTARDJA			
	09/920,240		ROO			08-01-01
PP	6,775,529	08-10-04	ROO			
	09/920,241		SUTARDJA			08-01-01
PP	6,844,837	01-18-05	SUTARDJA			

**EXAMINER**

Pyrene

**DATE CONSIDERED**

1/13/05

**\*EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE		ATTORNEY DOCKET NO.	APPLICATION NO.
		MP0020	09/737,743
<b>LIST OF REFERENCES CITED BY APPLICANT</b>		APPLICANT	
DATE SUBMITTED TO USPTO: August 11, 2005		Sehat SUTARDJA	
		FILING DATE	GROUP
		12/18/2000	2631
<b>OTHER DOCUMENTS</b> (Including author, title, date, pertinent pages, etc.)			
*EXAMINER INITIALS			
	Rao, Short Course: Local Area Networks		
	Razavi, Principles of Data Conversion System Design		
	Mano, Digital Logic and Computer Design		
	Farjad-rad, et al., 4.5 A 0.2-2GHz 12mW Multiplying DLL for Low-Jitter Clock Synthesis in Highly Integrated Data Communication Chip		
	Gotoh, et al., All-Digital Multi-Phase Delay Locked Loop for Internal Timing Generation in Embedded and/or High-Speed DRAMS		
	Johnson, et al., THAM 11.2: A Variable Delay Line Phase Locked Loop for CPU-Coprocessor Synchronization		
	Sonntag, et al., FAM: 11.5: A Monolithic CMOS 10MHz DPLL for Burse-Mode		
	Garlepp, et al., A Portable Digital DLL Architecture for CMOS Interface Circuits		
	Lin, et al., A Register-Controller Symmetrical DLL for Double-Data-Rate DRAM		
	Garlepp, et al., A Portable Digital DLL for High-Speed CMOS Interface Circuits		
	Dehng, et al., Clock-Deskaw Buffer Using a SAR-Controlled Delay-Locked Loop		
	Kim, et al., A Low-Power Small-Area 7.28-ps-Jitter 1-GHz DLL-Based Clock Generator		
	Dehng, et al., A Fast-Lock Mixed-Mode DLL Using a 2-b SAR Algorithm		
	Lin, et al., A 10-b, 500-Msample/s CMOS DAC in 0.6mm2		
EXAMINER	pylm	DATE CONSIDERED	9/13/05
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			